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Low Power Scan-based Built-in Self-test Based on True Random Number Generator Using Multistage Feedback Ring Oscillator

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ABSTRACT

A new low power scan-based built-in self-test (BIST) technique is proposed based on weighted pseudorandom test pattern generation and reseeding. A new LP scan architecture is proposed, which supports both pseudorandom testing and deterministic BIST. During the pseudorandom testing phase, an LP weighted random test pattern generation scheme is proposed by disabling a part of scan chains. During the deterministic BIST phase, the design for testability architecture is modified slightly while the linear feedback shift register is kept short. In both the cases, only a small number of scan chains are activated in a single cycle. Sufficient experimental results are presented to demonstrate the performance of the proposed LP BIST approach. This Proposed design will be implemented by Verilog HDL and simulated by Modelsim Tool.

Keywords: Built-in; Self-test; Linear Feedback Shift Register; Verilog HDL.

1. Introduction

The gap between functional and test power consumption is growing bigger and bigger, with the latter reaching 2X to 5X of the former due to the ever-shrinking functional power and ever-increasing test power. Problems, such as excessive heat that may reduce circuit reliability, formation of hot spots, difficulty in performance verification, reduction of the product yield and lifetime, and so on, have become severe. A fast simulation approach was proposed for low-power (LP) off-chip interconnect design. An important through silicon via (TSV) modeling/ simulation technique for LP 3-D stacked IC design.

Furthermore, the power dissipation of scan-based built-in self-test (BIST) is much higher than power dissipation in deterministic scan testing due to excessive switching activities caused by random patterns. Therefore, it is essential to propose an effective LP BIST approach. However, many of the previous LP BIST approaches cause fault coverage loss to some extent. Therefore, achieving high fault coverage in an LP BIST scheme is also very important. Weighted pseudorandom testing schemes and methods can effectively improve fault coverage.

However, these approaches usually result in much more power consumption due to more frequent transitions at the scan flip flops in many cases. Therefore, we intend to propose an LP scan-based pseudo random pattern generator (PRPG).

Bit-Swapping LFSR and Scan-Chain Ordering [1] describes Novel Technique for Peak- and Average-Power Reduction in Scan-Based BIST. This paper presents a novel low-transition linear feedback shift register (LFSR) that is based on some new observations about the output sequence of a conventional LFSR. The proposed design, called bit-swapping LFSR (BS-LFSR), is composed of an LFSR and a 2 × 1 multiplexer. When used to generate test patterns for scan-based built-in self-tests, it reduces the number of transitions that occur at the scan-chain input during scan shift operation by 50% when compared to those patterns produced by a conventional LFSR. Hence, it

reduces the overall switching activity in the circuit under test during test applications. The BS-LFSR is combined with a scan-chain-ordering algorithm that orders the cells in a way that reduces the average and peak power (scan and capture) in the test cycle or while scanning out a response to a signature analyzer. These techniques have a substantial effect on average- and peak-power reductions with negligible effect on fault coverage or test application time [2-11].

Scan Test Cost and Power Reduction through Systematic Scan Reconfiguration [3] describes presents segmented addressable scan (SAS), a test architecture that addresses test data volume, test application time, test power consumption, and tester channel requirements using a hardware overhead of a few gates per scan chain [12-21]. Using SAS, this paper also presents systematic scan reconfiguration, a test data compression algorithm that is applied to achieve 10× to 40× compression ratios without requiring any extra information from the automatic-test-pattern- generation tool about the unspecified bits.

Efficient Scan Tree Design [25] describes tree-based scan path architectures have recently been suggested for reducing test application time or test data volume in today's high-density very large-scale integrated circuits. However, these techniques strongly rely on the existence of a large number of compatible sets of flip-flops under the given test set and therefore may not be suitable for a highly compact test set generated by an efficient automatic test pattern generator tool. Tree-based architectures also suffer from loss of fault coverage while achieving a significant reduction ratio for test time or data.

To circumvent this problem, a new two-pass hybrid method is proposed to design an efficient scan tree architecture based on approximate compatibility. The method is particularly suitable for a highly compact test set having fewer don't cares and low compatibility. Finally, to reduce the volume of scan-out data, test responses shifted out from the leaf nodes of the scan tree are compacted by a space compactor, which is designed especially for the proposed scan tree architecture. The compactor uses an XOR tree, and its overhead is low.

A BIST Pattern Generator Design [7] describes a new design methodology for a pattern generator is proposed, formulated in the context of on-chip BIST. The design methodology is circuit-specific and uses synthesis techniques to design BIST generators. The pattern generator consists of two components: a pseudorandom pattern generator (like an LFSR or, preferably, a GLFSR) and a combinational logic to map the outputs of the pseudorandom pattern generator. This combinational logic is synthesized to produce a given set of target patterns by mapping the outputs of the pseudorandom pattern generator.

It is shown that, for a particular CUT, an area-efficient combinational logic block can be designed/synthesized to achieve 100 (or almost 100) percent single stuck-at fault coverage using a small number of test patterns. This method is significantly different from weighted pattern generation and can guarantee testing of all hard-to-detect faults without expensive test point insertion. Experimental results on common benchmark netlists demonstrate that the fault coverage of the proposed pattern generator is significantly higher compared to conventional pattern generation techniques [22-24]. The design technique for the logic mapper is unique and can be used effectively to improve existing pattern generators for combinational logic and scan-based BIST structures.

Low-Power Programmable PRPG [9] describes a low-power (LP) programmable generator capable of producing pseudorandom test patterns with desired toggling levels and enhanced fault coverage gradient compared with the best-to-date built-in self-test (BIST)- based pseudorandom test pattern generators. It is comprised of a linear finite state machine (a linear feedback shift register or a ring generator) driving an appropriate phase shifter, and it comes with a number of features allowing this device to produce binary sequences with preselected toggling (PRESTO) activity.

We introduce a method to automatically select several controls of the generator offering easy and precise tuning. The same technique is subsequently employed to deterministically guide the generator toward test sequences with improved fault-coverage-to pattern- count ratios. Furthermore, this paper proposes an LP test compression method that allows shaping the test power envelope in a fully predictable, accurate, and flexible fashion by adapting the PRESTO-based logic BIST (LBIST) infrastructure. The proposed hybrid scheme efficiently combines test compression with LBIST, where both techniques can work synergistically to deliver high quality tests.

1.1. Objective

A new LP scan architecture is proposed, which supports both pseudorandom testing and deterministic BIST. During the pseudorandom testing phase, an LP weighted random test pattern generation scheme is proposed by disabling a part of scan chains. To improve the low power scan based by using Xilinx and modelsim.

Section 2 provides a Low power scan-based built-in self-test. Section 3 is about the Result and Discussion and Sections 4 and 5 is about Conclusion and Future works.

2. True Random Number Generator Based on Multistage Feedback Ring Oscillator

Weighted pseudorandom testing schemes can effectively improve fault coverage. A weighted test-enable signal-based pseudorandom test pattern generation scheme was proposed for scan-based BIST, according to which the number of shift cycles and the number of capture cycles in a single test cycle are not fixed. Reconfigurable scan architecture was used for the deterministic BIST arrangement using the weighted test enable signal-based pseudo-random test generation scheme. Proposed a new scan segmentation approach for more effective BIST.

The PLL generates two normal clocks. The output of PLL is used as the data input of flip-flop, and the output of MSFRO is used as the clock signal input of flip-flop. Each time the rising edge of the MSFRO output signal comes, the D flip-flop will sample the PLL output signal to generate one random bit. The phase jitter range caused by noise is very small, and many definite values will be sampled when using the trigger to sample, which will reduce the randomness of random numbers. Therefore, the proposed TRNG uses two MSFRO as the entropy source, and directly obtains random numbers by XOR output after extracting their randomness.

2.1. Low Power Scan-Based Self-Based on Weighted Pseudo Random Test Pattern

we propose a new LP scan-based BIST architecture, which supports LP pseudorandom testing, LP deterministic BIST and LP reseeding. We present the major contributions of this paper in the following.

A new LP weighted pseudorandom test pattern generator using weighted test-enable signals is proposed using a new clock disabling scheme. The design-for testability (DFT) architecture to implement the LP BIST scheme is

presented. Our method generates a series of degraded sub circuits. The new LP BIST scheme selects weights for the test-enable signals of all scan chains in each of the degraded sub circuits, which are activated to maximize the testability. A new LP deterministic BIST scheme is proposed to encode the deterministic test patterns for random pattern- resistant faults.

Only a part of flip flops are activated in each cycle of the whole process of deterministic BIST. A new procedure is proposed to select a primitive polynomial and the number of extra variables injected into the linear-feedback shift register (LFSR) that encode all deterministic patterns. The new LP reseeding scheme.

2.2. Architecture

BIST is basically same as off-line testing using ATE where the test pattern generator and the test response analyzer are on-chip circuitry (instead of equipments). As equipments are replaced by circuitry, so it is obvious that compressed implementations of test pattern generator and response analyzer are to be designed.

This module generates the test patterns required to sensitize the faults and propagate the effect to the outputs (of the CUT). As the test pattern generator is a circuit (not equipment) its area is limited. So, storing and then generating test patterns obtained by ATPG algorithms on the CUT (discussed in Module XI) using the hardware test pattern generator is not feasible. In other words, the test pattern generator cannot be a memory where all test patters obtained by running ATPG algorithms (or random pattern generation algorithms) on the CUT are stored and applied during execution of the BIST.

This multiplexer is to allow normal inputs to the circuit when it is operational and test inputs from the pattern generator when BIST is executed. The control input of the multiplexer is fed by a central test controller. Output response compacter performs lossy compression of the outputs of the CUT. As in the case of off-line testing, in BIST the output of the CUT is to be compared with the expected response (called golden signature); if CUT output does not match the expected response, fault is detected. Similar to the situation for test pattern generator, expected output responses cannot be stored explicitly in a memory and compared with the responses of the CUT. So, CUT response needs to be compacted such that comparisons with expected responses (golden signatures) become simpler in terms of area of the memory that stores the golden signatures.

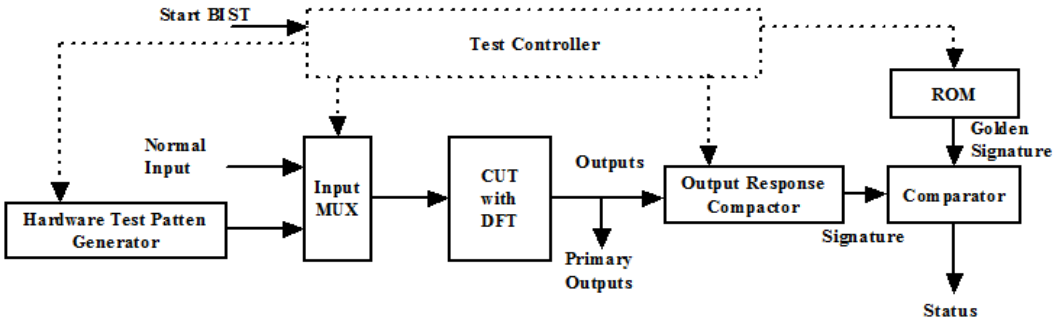

Figure 2.1. Basic Architecture of BIST

Circuit to control the BIST. Whenever an IC is powered up (signal start BIST is made active) the test controller starts the BIST procedure. Once the test is over, the status line is made high if fault is found. Following that, the

controller connects normal inputs to the CUT via the multiplexer, thus making it ready for operation. Among the modules discussed above, the most important ones are the hardware test pattern generator and the response compactor. In the next two sections we will discuss these two blocks in details.

The conventional design of the MISR incorporates a feedback shift register which forms the signature of n-inputs in parallel. The theory of its operation can be stated simply as follows. An n-bit input (one from each input line) is added, modulo 2, to the contents of the n-D-flip-flops (constituting the register). The result is shifted one position before the next word is added. After the last input bit is added, the remaining contents of the D-flip-flops are the aggregated output signature.

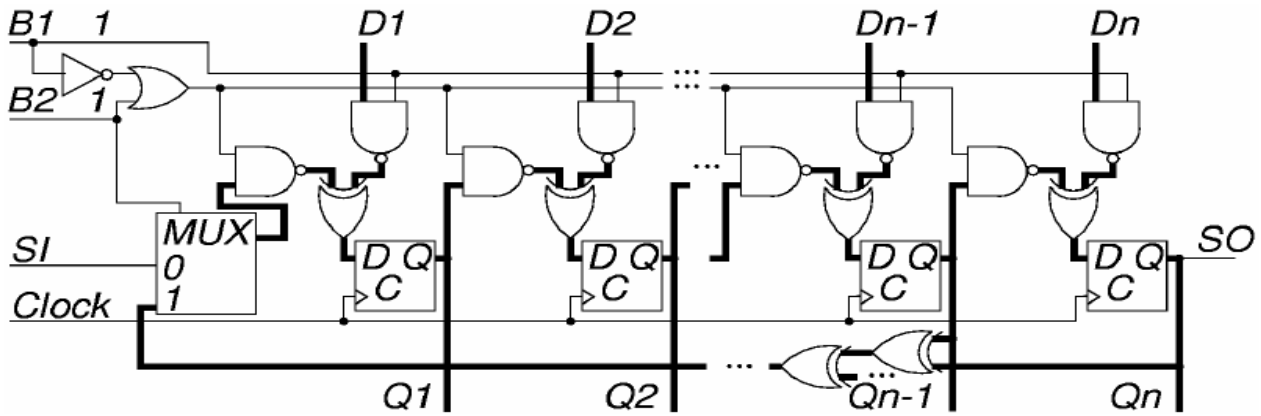

Figure 2.2. Multiple Input Signature Register

Scan chains are the elements in scan-based designs that are used to shift-in and shift-out test data. A scan chain is formed by a number of flops connected back to back in a chain with the output of one flop connected to another. The input of first flop is connected to the input pin of the chip (called scan-in) from where scan data is fed. The output of the last flop is connected to the output pin of the chip (called scan-out) which is used to take the shifted data out. The figure below shows a scan chain.

Figure 2.3. Scan chain

3. Results

Snapshot is nothing but every moment of the application while running. It gives the clear elaborated of application. It will be useful for the new user to understand for the future steps.

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Various Snapshots

TRND Initial Wave

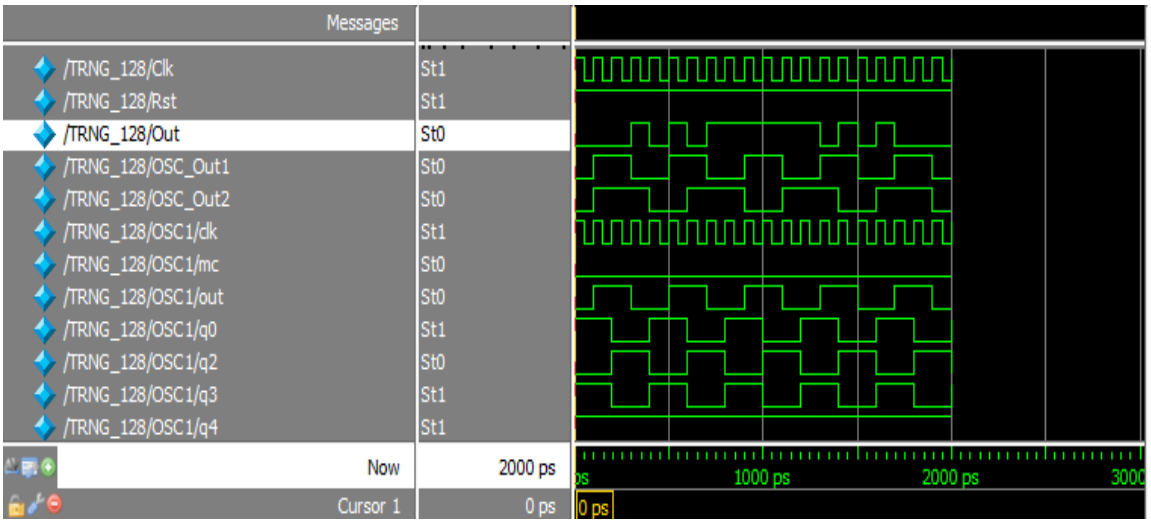

Figure 3.1. TRND initial wave

TRNG 128 Bit

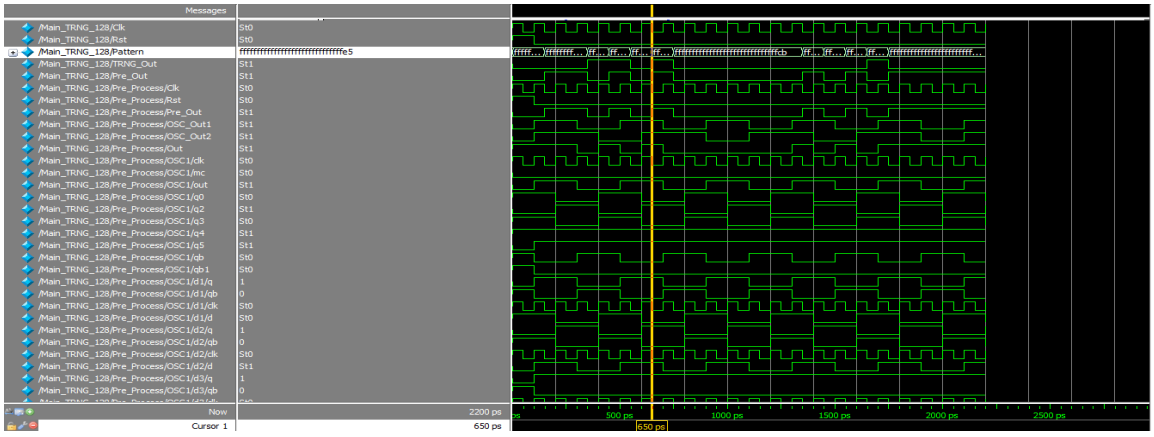

Figure 3.2. TRNG 128 bit wave

TRNG Pre Block

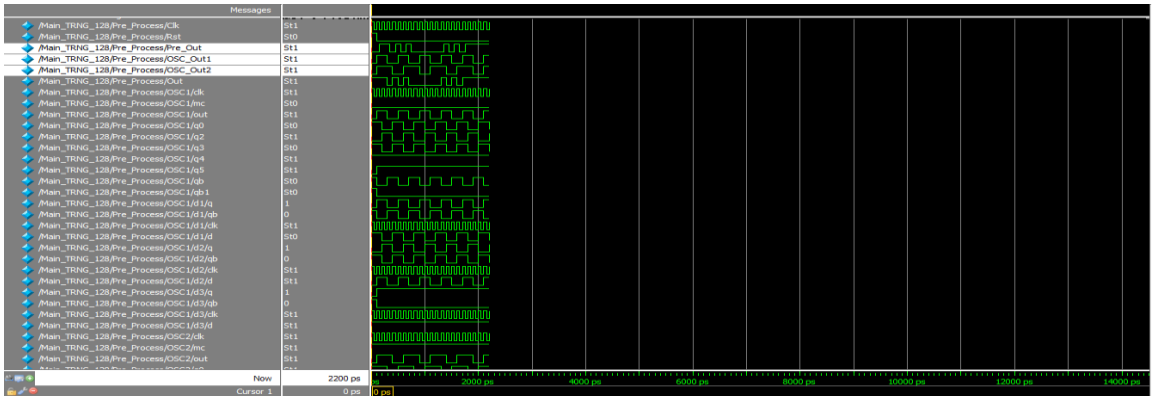

Figure 3.3. TRND pre block

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LP Logic Code

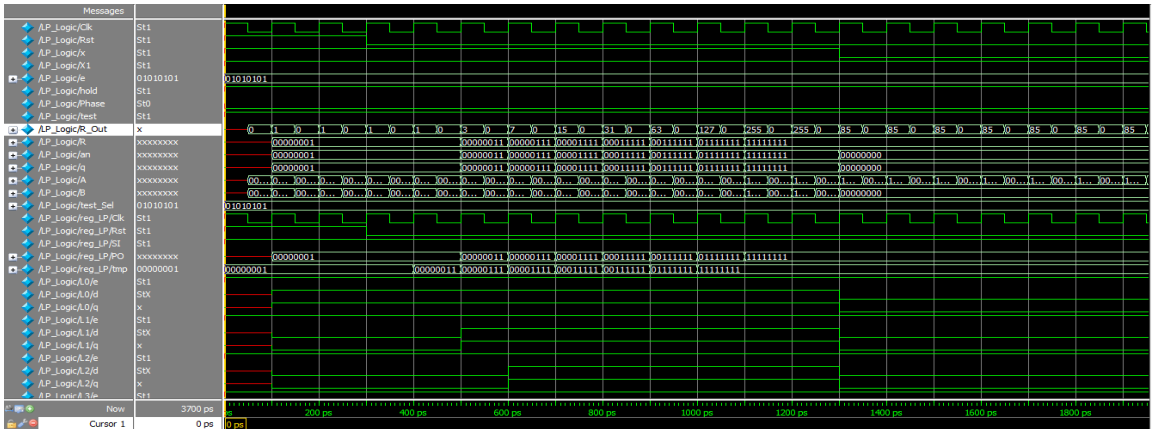

Figure 3.4. LP logic code

Scan Chain New

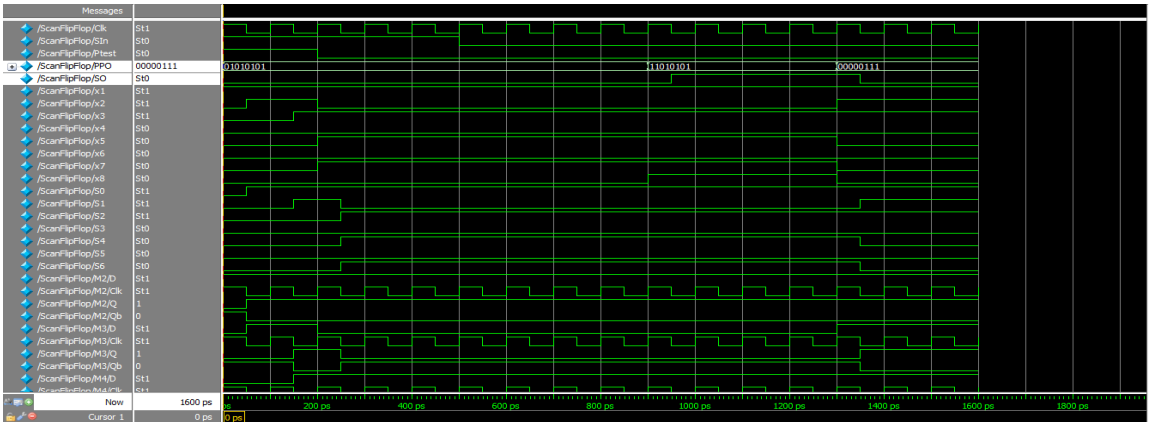

Figure 3.5. Scan chain new

Device Utilization Summary

Table 3.1. Device utilization summary

Device Utilization Summary				
Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Total Number Slice Registers	48	3,840	1%	
Number used as Flip Flops	40			
Number used as Latches	8			
Number of 4 input LUTs	88	3,840	2%	
Logic Distribution				
Number of occupied Slices	67	1,920	3%	
Number of Slices containing only related logic	67	67	100%	
Number of Slices containing unrelated logic	0	67	0%	
Total Number of 4 input LUTs	96	3,840	2%	
Number used as logic	88			
Number used as a route-thru	8			
Number of bonded IOBs	49	97	50%	
IOB Flip Flops	8			
Number of GCLKs	3	8	37%	
Total equivalent gate count for design	1,024			
Additional JTAG gate count for IOBs	2,352			

4. Conclusion

A new LP BIST method has been proposed using weighted test-enable signal-based pseudorandom test pattern generation and LP deterministic BIST and reseeding. The new method consists of two separate phases: 1) LP weighted pseudorandom pattern generation and 2) LP deterministic BIST with reseeding. The first phase selects weights for test-enable signals of the scan chains in the activated sub circuits.

5. Future Work

A new procedure has been proposed to select the primitive polynomial and the number of extra inputs been proposed to further reduce test data kept on-chip. Experimental results have demonstrated the performance of the proposed method by comparison with a recent LP BIST method. The LP reseeding technique is a little more complicated. This work can be extended to latch-on-capture transition fault testing and small delay defect.

Declarations

Source of Funding

This study has not received any funds from any organization.

Conflict of Interest

The authors declare that they have no conflict of interest.

Consent for Publication

The authors declare that they consented to the publication of this study.

Authors' Contribution

All the authors took part in literature review; research; and manuscript writing equally.

References

[1] Jay Kumar S.R., Arivazhagan P., Saranya K., & Manikandaprabu N. (2014). Genetic Algorithm based test Pattern Generation for Asynchronous Circuits with Handshake Controllers. Unique Journal of Engineering and Advanced Sciences, 2(1).

[2] Abu-Issa A.S., & Quigley S.F. (2009). Bit-swapping LFSR and scan-chain ordering: A novel technique for peak- and average-power reduction in scan-based BIST. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst., 28(5): 755–759.

[3] Agrawa V.D., Kime C.R., & Saluja K.K. (1993). A tutorial on built-in self-test. I. Principles. IEEE Des. Test Comput., 10(1): 73–82.

[4] Al-Yamani A., Devta-Prasanna N., Chmelar E., Grinchuk M., & Gunda A. (2007). Scan test cost and power reduction through systematic scan reconfiguration. IEEE Trans. Comput. Aided Des. Integrated Circuits Syst., 26(5): 907–918.

[5] Bardell P.H., Mc Anney W.H., & Savir J. (1987). Built in Test for VLSI: Pseudorandom Techniques. New York, NY, USA, Wiley.

[6] Bushnell M., & Agrawal V.D. (2000). Essentials of Electronic Testing. Norwell, MA, USA, Kluwer.

[7] Brglez F., Pownall P., & Hum P. (1984). Applications of testability analysis: From ATPG to critical path tracing. In Proc. IEEE Int. Test Conf., Pages 705–712.

[8] Chatterjee M., & Pradhan D.K. (2003). A BIST pattern generator design for near-perfect fault coverage. IEEE Trans. Comput., 52(12): 1543–1558.

[9] Chen D. Xiang & Yin B. (2009). The ATPG conflict-driven scheme for high transition fault coverage and low-test cost. In Proc. 27th IEEE VLSI Test Symp., Pages 146–151.

[10] Filipek M. et al. (2015). Low-power programmable PRPG with test compression capabilities. IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 23(6): 1063–1076.

[11] Gerstendörfer S., & Wunderlich H.J. (1999). Minimized power consumption for scan-based BIST. J. Electron. Test., 16(3): 203–212.

[12] Girard P., Landrault C., Pravossoudovitch S., Virazel A., & Wunderlich H.J. (2002). High defect coverage with low-power test sequences in a BIST environment. IEEE Des. Test Comput., 21(5): 44–52.

[13] Girard P., Guiller L., Landrault C., & Pravossoudovitch S. (2000). Low power BIST design by hypergraph partitioning: Methodology and architectures. In Proc. Int. Test Conf., Pages 652–661.

[14] Hellebrand S., Rajski J., Tarnick S., Venkataraman S., & Courtois B. (1995). Built-in test for 8circuits with scan based on reseeding of multiple polynomial linear feedback shift registers. IEEE Transactions on Comput., 44(2): 223–233.

[15] Hellebrand S., Liang H.G., & Wunderlich H.J. (2000). A mixed mode BIST scheme based on reseeding of folding counters. In Proc. Int. Test Conf., Pages 778–784.

[16] Huang Y., Pomeranz I., Reddy S.M., & Rajski J. (2000). Improving the proportion of at-speed tests in scan BIST. In Proc. IEEE/ACM Int. Conf. Comput. Aided Design, Pages 459–463.

[17] Jinkyu Lee & Nur A. Touba (2010). Adaptive Low Shift Power Test Pattern Generator for Logic BIST. In Proc. IEEE/ACM Int. Conf. Comput. Aided Design, Pages 149–154.

[18] Jinkyu Lee & Nur A. Touba (2007). LFSR-Reseeding Scheme Achieving Low-Power Dissipation During Test. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst., 26(7): 1331–1339.

[19] Jiang Z., Xiang D., & Shen K. (2015). A novel scan segmentation design for power controllability and reduction in at-speed test. In Proc. Asian Test Symp., Page 19.

[20] Jiang Z., Xiang D., & Shen K. (2015). A scan segmentation architecture for power controllability and reduction. In Proc. 28th Int. Conf. SOCC, Pages 269–274.

[21] Kiefer G., & Wunderlich H.J. (1999). Deterministic BIST with multiple scan chains. J. Electron. Test., 14(1): 85–93.

[22] Lei Li & Krishnendu C. (2004). Test Set Embedding for Deterministic BIST Using a Reconfigurable Inter connection Network. IEEE Trans. Very Large Scale Integr. (VLSI) Syst., 12(12): 1277–1283.

[23] Mehrdad Nourani & Mohammad Tehranipoor (2010). Low-Transition Test Pattern Generation for BIST-Based Applications. In Proc. 28th IEEE VLSI Test Symp., Pages 141–146.

[24] Omaria M. (1996). Novel Approach to Reduce Power Droop During Scan-Based Logic BIST. IEEE Trans. Comput. Aided Des. Integr. Circuits Syst., 15(8): 1020–1025.

[25] Shibaji Banerjee & Dipanwita Roy Chowdhury (2003). An Efficient Scan Tree Design for Compact Test Pattern Set. J. Electron. Test. Theory Appl., 19(6): 637–644.